UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,675	04/14/2004	Robert O. Conn	X-1322-1-1D US	8082

24309 7590 02/03/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,675	CONN, ROBERT O.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-14-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. This application appears to be a division of Application No. 10/407,746, filed April 04, 2003 which is issued as U.S.Patent 6,753,239. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application.

Information Disclosure Statement

2. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field April 14, 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims **1-2 & 5-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (US 4,980,308).

Re claim **1**, Hayashi teaches an integrated circuit die, comprising (Fig.2):

a device wafer portion having a face side surface, the device wafer portion comprising a semiconductor wafer portion and an interconnect portion, the interconnect portion having a surface that is the face side surface of the device wafer, the semiconductor wafer portion comprising a source region (35sa) of a first conductivity type (P+) and a drain region (35da) of the first conductivity type (P+) and a channel structure of a second conductivity (N-) type opposite the first conductivity type, wherein the source region, the drain region and the channel structure are part of a single layer of a semiconductor material and together form an island of the semiconductor material; and a supporting structure portion (1) that is bonded to the face side surface of the device wafer portion.

Re claim **2**, Hayashi teaches the island of semiconductor material has a substantially planar bottom surface, the source region having a bottom surface that makes up a part of the substantially planar bottom surface of the island, the drain region having a bottom surface that makes up another part of the substantially planar bottom surface of the island, wherein the planar bottom surfaces of the source and drain regions are not in contact with any semiconductor material of the semiconductor wafer portion of the device wafer (See Fig.2B).

Re claim **5**, Hayashi teaches the semiconductor wafer portion of the device wafer comprises a plurality of islands, each of the islands comprising a source region, a drain region, and a channel structure.

Re claim **6**, Hayashi teaches the source region has a substantially no junction capacitance other than a junction capacitance between the source region and a channel structure.

Re claim **7**, Hayashi teaches the island consists essentially of the source region, the drain region and the channel structure.

Re claims **8**, Hayashi teaches a transistor structure, comprising (Fig.2):

a device wafer having a substantially planar face side, the device wafer comprising:

a gate (34A); a source region (35sa); a drain region (35da); and means (channel) for providing a conductive channel between the source region and the drain region such that substantially the only junction capacitance on the source region is junction capacitance due to interface between the source region and the means (Fig.2B); and a supporting structure (1) that I wafer-bonded to the face side of the device wafer.

Re claim **9**, Hayashi teaches the device wafer comprises an island of semiconductor material, and wherein the island of semiconductor material consists essentially of the source region, the drain region, and the means (channel).

5. Claims **1 & 4** are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa (US 6,682,963).

Re claim **1**, Ishikawa teaches an integrated circuit die, comprising (Fig.9A-10C):

a device wafer portion having a face side surface, the device wafer portion comprising a semiconductor wafer portion and an interconnect portion, the interconnect

portion having a surface that is the face side surface of the device wafer, the semiconductor wafer portion comprising a source region of a first conductivity type and a drain region of the first conductivity type and a channel structure of a second conductivity type opposite the first conductivity type, wherein the source region, the drain region and the channel structure are part of a single layer of a semiconductor material and together form an island of the semiconductor material; and a supporting structure portion (419) that is bonded to the face side surface of the device wafer portion. See Col.20, line 21-Col.21, line 67.

Re claim **4**, Ishikawa teaches the supporting structure is a semiconductor wafer that is wafer-bonded to the face side surface of the device wafer portion (Col.20, line 66-Col.21, line 2).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **3 & 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (US 4,980,308) in view of Matsumoto et al. (US 6,794,717).

Hayashi teaches substantially the claimed structure as explained claims 1 & 8 above, except that the channel structure has a key-shape. Matsumoto teaches in Fig.9 the channel structure has a key-shape. This key-shape may reduce an area covering an edge of an active region hence a gate capacitance can be reduced. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to form key-shape channel structure as taught by Matsumoto in Hayashi's device since this key-shape channel reduce area covering an edge of an active region so as to reduce gate capacitance.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Han et al. (US 6,033,925)

Takemura et al. (US 5,786,242)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk